Quik VOICE

VP-1000A
Digital Voice Processor

FEATURES

- High quality voice & sound generation
- Record & playback with external SRAM
- Playback-only with external EPROM or ROM
- Stand-alone operation
- 32K x 8 direct memory addressing, expandable
- Single 5V DC supply voltage
- Low power consumption
- Continuous Variable Slope Delta (CVSD) modulation
- Sampling rate from 24Kbps to 128 Kbps
- Message digitization with the VP-880 or the VW-1000A
- Pin to pin compatible with UM5100
- 40-pin DIP (VP-1000A) or 48-pin LQFP (VP-1000AFL)

GENERAL DESCRIPTIONS

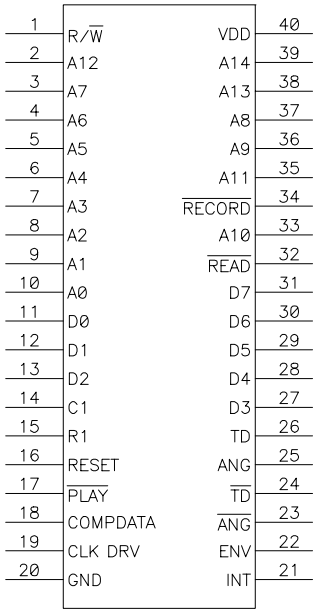
The VP-1000A is an advanced CMOS LSI chip for general purpose voice/sound record and playback applications. It can be interfaced with external SRAM to construct a realtime recording circuitry, or with external ROM or EPROM for playback only applications. When ROM or EPROM is used, the sound must be digitized by using Eletech's VP-880 Voice Development System or VW-1000A Voice EPROM Writer.

The VP-1000A is totally self-contained. It can access the external memory all by itself without the help from any microprocessor. Although the chip provides only 15 address lines, an external counter can be easily added to extend the memory addressing to virtuely no limitation. Therefore very long message length can be achieved easily. Overall, the VP-1000A offers high voice quality and flexible memory addressing that no other chips can.

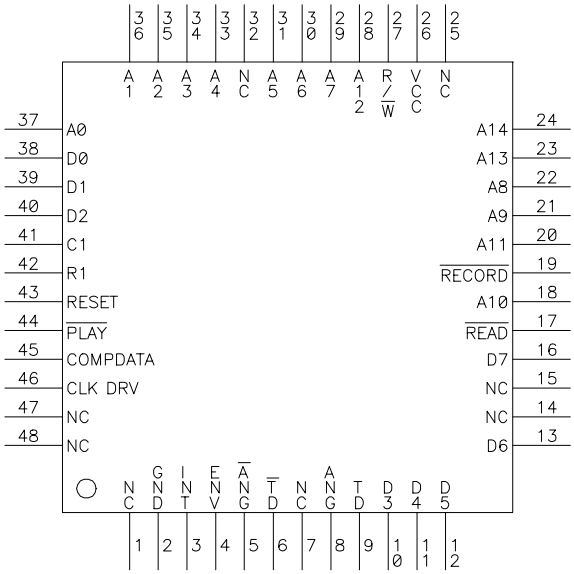
APPLICATIONS

- Voice memo recorder
- Sound effects generator
- Digital announcer for consumer, industrial, security and telecommunication products

VP-1000A (DIP40) Pin Assignment



VP-1000AFL (LQFP48) Pin Assignment



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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, V_{DD} - V_{SS} ..... 0 to 5.5V
Input Volotage, V_{IN} ..... V_{SS} to V_{DD}
Operating Temperature, T_{OP} ..... -10°C to 60°C
Storage Temperature, T_{ST} ..... -20°C to 80°C

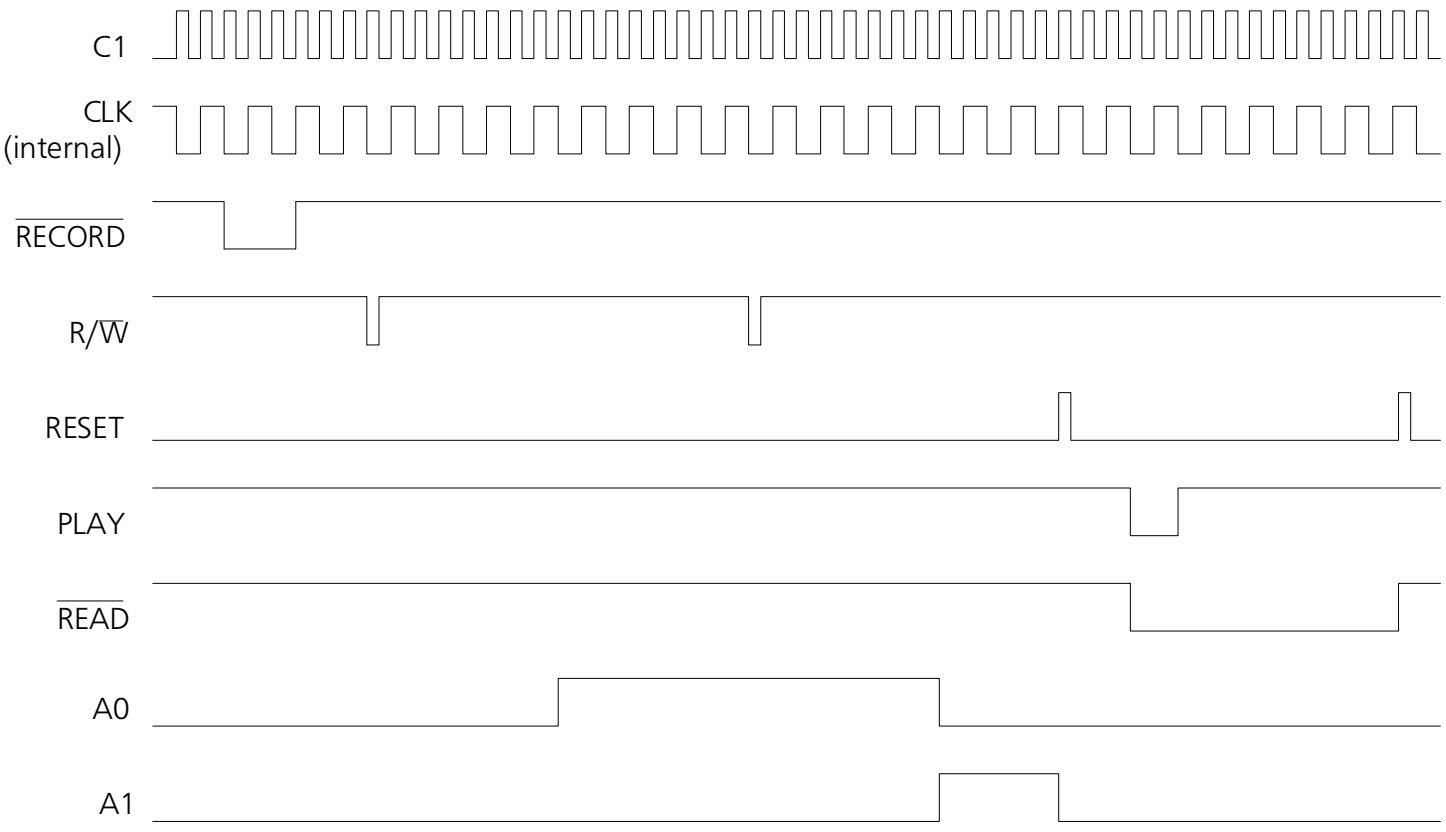
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, F_{OSC} = 64KHz, F_{CLOCK} = 32 KHz unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DD}	Standby Current			50		uA
I_{DRIVE}	Clock Drive Current		16			mA
I_{SINK}	Clock Sink Current		16			mA
V_{IH}	Input	High	3.5		5	V
V_{IL}	Voltage	Low	0		1.5	V
I_{DRIVE}	Output	Drive	3	4		mA
I_{SINK}	Current	Sink	3	4		mA
T_{RESET}	Reset Pulse Width		500			ns
T_{WRITE}	Write Pulse Width		200			ns
S/N	Signal-to-Quantizied Noise Ratio			30		dB

TIMING DIAGRAM



PIN DESCRIPTIONS

A0 - A14
Output, address bus, expandable by adding a counter.

ANG & $\overline{\text{ANG}}$
Output, differential analog audio signal.

C1
Input, internal RC oscillator. If external clock is to be used, it must be connected to this pin and its frequency twice as fast as the sampling rate.

CLK DRV
Output, a square wave of the same frequency as the sampling rate when the chip is in the Record or the Play mode. The frequency will be lower when the chip is in the Idle mode.

COMPDATA
Input, feedback from the external comparator output.

D0 - D7
Input/output, data bus.

ENV
Input, to be connected to an external integrator output.

INT
Output, connected to an external integrator to produce envelope waveform.

GND
Ground.

$\overline{\text{PLAY}}$
Input, active low. When the chip is idle but not under reset, pulsing this pin will put the chip in the Play mode.

R1
Output, internal RC oscillator. Leave un-connected when using external clock.

$\overline{\text{READ}}$
Output, active low. It indicates the chip is in the Play mode. This signal is usually used to enable memory output.

$\overline{\text{RECORD}}$
Input, active low. When the chip is idle but not under reset, pulsing this pin will put the chip in the Record mode.

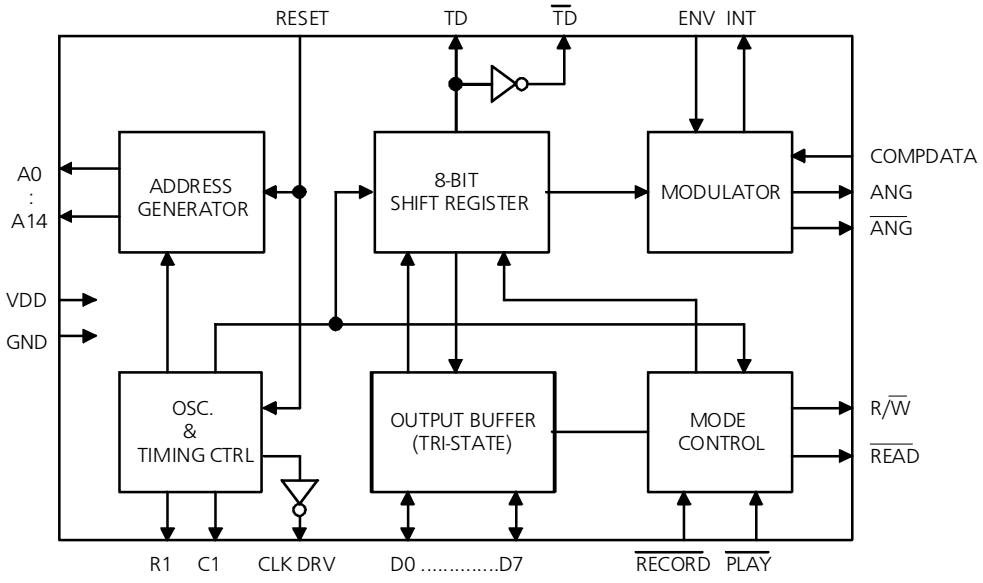
RESET
Input, active high. Reset the chip back to the Idle mode. This pin is level sensitive.

R/$\overline{\text{W}}$
Output, active low. This pin generates a pulse each time the clock counts to eight. It is usually used as a write strobe for the SRAM. Active only in the Record mode.

TD, $\overline{\text{TD}}$
Output, for signal modulation. These pins are useful in the Record mode only.

VDD
Input, supply voltage.

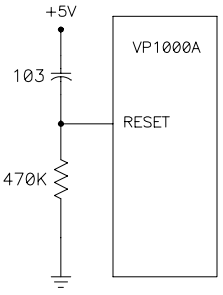
Block Diagram



APPLICATION NOTES

1. Reset Consideration

The Reset pin should never be left floating. If the Reset pin is not controlled by a non-floating signal, use the following Reset circuitry. Note that the 0.01uF capacitor is added so that the VP-1000A gets a Reset pulse on power-up.



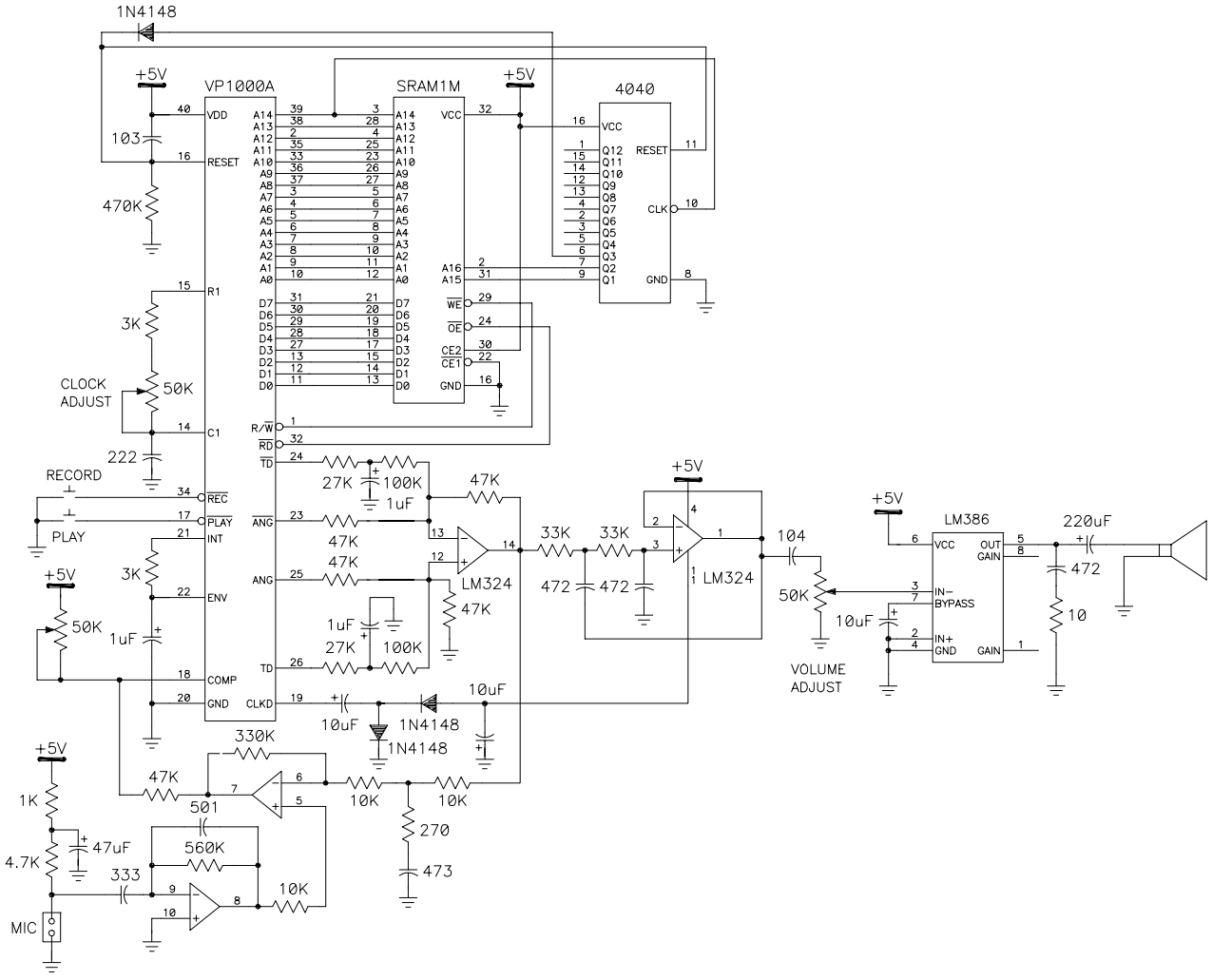
RECOMMENDED VP1000A
RESET CIRCUITRY

2. Memory Address Expansion

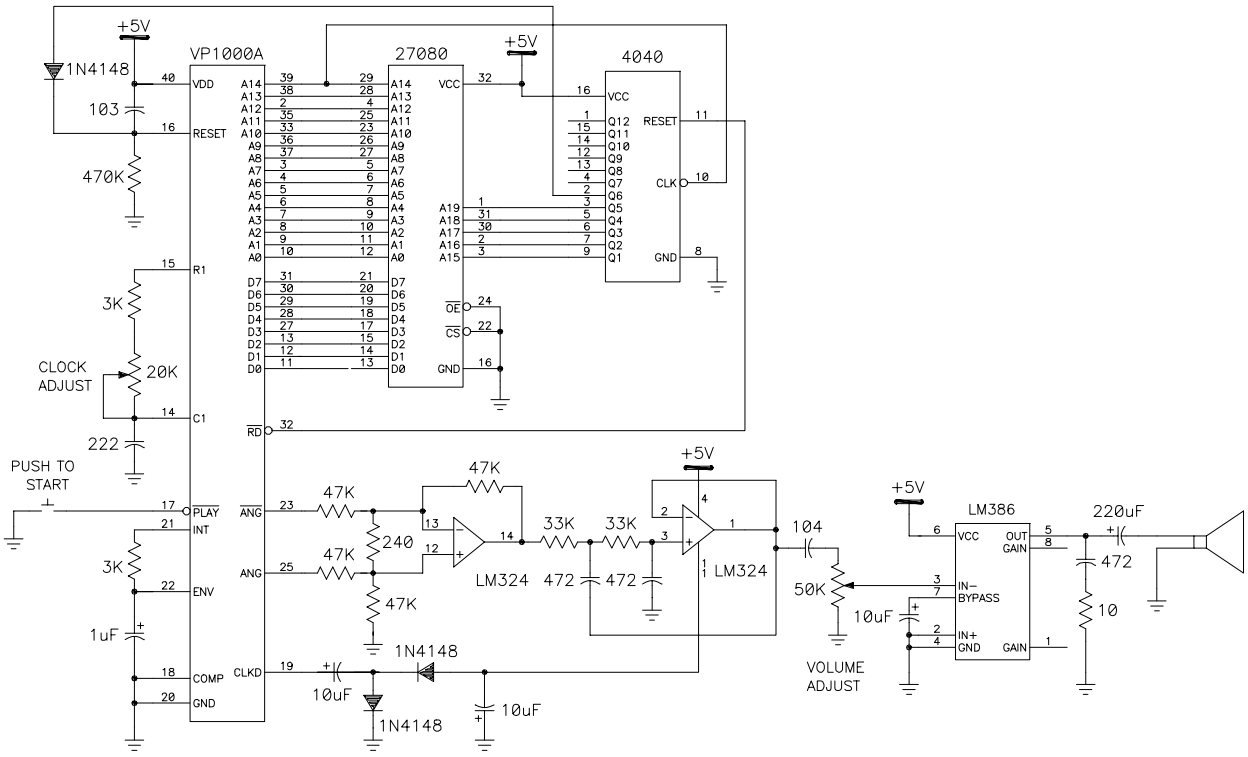
The VP-1000A's internal 15-bit address counter covers memory space up to 32K x 8, or 256K bits. It can be easily expanded by just adding a binary counter, clocked by the falling edge of address line A14. The first counter output becomes A15, the second output becomes A16 and etc. This is possible since once started, the VP-1000A will not stop recording or playing until it is reset. When the internal counter reaches the maximum count, it simply overflows and restarts from zero again. Therefore the VP-1000A can access an unlimited amount of memory.

CIRCUIT DESIGN EXAMPLES

1. Single-Message Record and Play, 1M SRAM

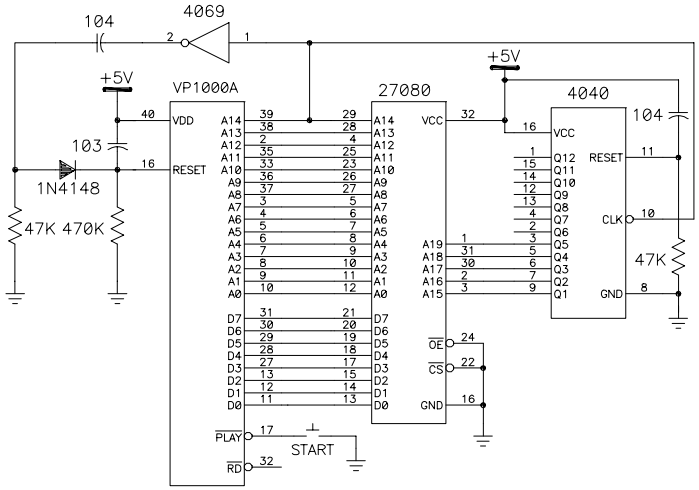


2. Single-Message Playback, 8M EPROM



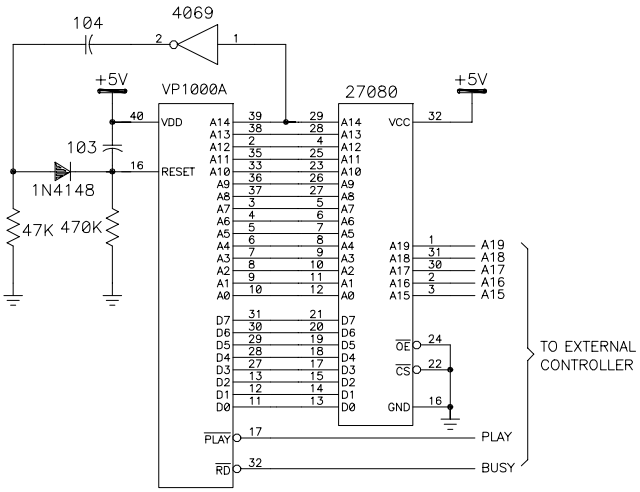
3. Multiple-Message Playback, Sequential Control

The 8M EPROM is divided into 32 equal segments of 256K bits. Each message is stored in such a segment and must be 256K bits or smaller. The first trigger will activate only the first segment. The next trigger will activate the next segment, and etc.

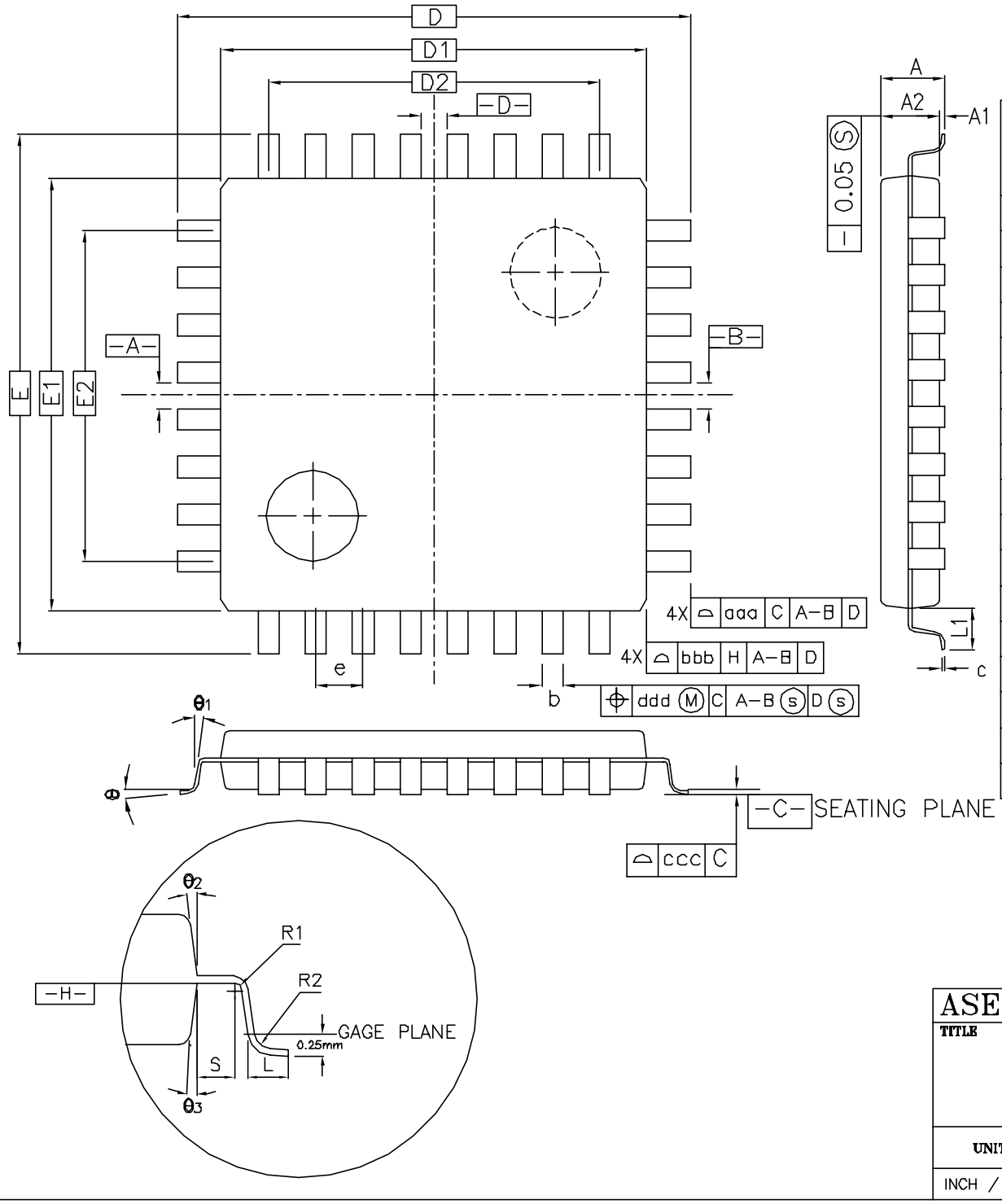


4. Multiple-Message Playback, Controller Interface

The 8M EPROM is divided into 32 equal segments of 256K bits. Each message is stored in such a segment and must be 256K bits or smaller. The message is activated via a controller interface which consists of 5 address lines and a strobe signal (PLAY).



ASE ADVANCED SEMICONDUCTOR ENGINEERING,INC



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D_1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E_1	7.00 BSC.			0.276 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

ASE		SCALE: X	PROJ.
TITLE: PACKAGE OUTLINE 32/44/48L LQFP 7x7x1.40 mm 2.0mm FOOTPRINT		DWG. NO.: 64-06-280-1383	REV.: A
		SHEET: 1 OF 3	SIZE: A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
   MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE
   LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY
   MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS
   OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION
   AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and
   0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 44L WERE BASE ON THOSE OF 48L SINCE
   THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

ASE		SCALE: X	PROJ.
TITLE: PACKAGE OUTLINE 32/44/48L LQFP 7x7x1.40 mm 2.0mm FOOTPRINT		DWG. NO.: 64-06-280-1383	REV.: A
		SHEET: 2 OF 3	SIZE: A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

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REVISION HISTORY :

REV.	DESCRIPTION OF CHANGE	NAME	DATE
0	REGENERATE DRAWING INSTEAD OF 3450,3440 AND 3441(64-06-A000-PT01-D)	JANE SUN	03/31/00
	CHANGE DWG. NO FROM "02" TO "06".	JANE SUN	02/06/01
A	ADD *1 AND *2	AChen Yang	09/16/"02

ASE ADVANCED SEMICONDUCTOR ENGINEERING, INC.		DWG. NO.	REV.
TITLE: PACKAGE OUTLINE 32/44/48L LQFP 7x7x1.40 mm 2.0mm FOOTPRINT		64-06-280-1383	A
		SHEET	SIZE
		3 OF 3	A4

	DRAWN	CHECKED		APPROVED	
BY					
DATE					